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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/670,855	09/26/2000	John Michael Brown	20206-081 (TA-490)	6646

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EXAMINER

WHITTINGTON, ANTHONY T

ART UNIT PAPER NUMBER

2133

DATE MAILED: 02/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/670,855

Applicant(s)

BROWN, JOHN MICHAEL

Examiner

Anthony T Whittington

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 January 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7. 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Ruparel (U.S. 5,689,517).

As per claim 1, Ruparel teaches a digital circuit having at least first and second edge-triggered devices with first and second clock signals that includes all the elements of the instant application. Ruparel teaches the first and second edge-triggered devices (latch 11, latch 12) with first and second clock signals (CLK A, CLK B) in Figure 1a. Ruparel teaches a latch (latch 12a) in the scan data path that is equivalent to the instant application in Figure 1b.

As per claims 2, 3, and 4, Ruparel teaches multiplexer circuits (21a, 21b) for selectively forming the scan data path in response to a test signal (Data-in, SE) in Figure 2b. Ruparel teaches the first and second devices (latch 11, latch 12) form functional circuits in absence of the test signal in Figure 1a. Ruparel teaches the first and second clock signals (CK, ~CK) are asynchronous to one another in Figure 6a.

As per claim 5, Ruparel teaches a digital circuit subject to scan testing that comprises all the elements of the instant application. Ruparel teaches a scan data input (SCAN-IN), scan data output (SCAN-OUT), at least first and second clock domains (10a-10c), and a latch (latch 12a)

Art Unit: 2133

in a scan data path portion that is clocked by the second clock (CLK B) in Figure 1b. Ruparel teaches a selectable data path in response to a test signal (Data-in, SE) in Figure 2b.

As per claim 6, Ruparel teaches a method of scan testing digital logic that comprises all the elements of the instant application. Ruparel teaches the first and second edge-triggered devices (latch 11, latch 12) with first and second clock signals (CLK A, CLK B) in Figure 1a. Ruparel teaches the step for providing a latch element (latch, 11 a) in the data path clocked by a test clock and asserting a test signal (SCAN-IN) to cause at least one serial scan chain to be formed in Figure 1b. Ruparel teaches operating the first, second (CLK A, CLK B, Figure 1b), and test clock signal (SYSTEM_CLOCK, Figure 6a) to cause the scan chain to receive test data in Figure 2b.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of art with respect to edge triggered logic testing in general:

U.S. Pat No. 5,719,878 to Yu et al.

U.S. Pat No. 5,602,855 to Whetsel, Jr.

U.S. Pat No. 5,631,911 to Whetsel, Jr.

U.S. Pat No. 5,383,143 to Crouch et al.

U.S. Pat No. 5,717,700 to Crouch et al.

U.S. Pat No. 6,081,916 to Whetsel, Jr.

U.S. Pat No. 6,148,425 to Bhawmik et al.

U.S. Pat No. 6,467,044 to Lackey

Art Unit: 2133


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony T Whittington whose telephone number is 703-306-5617. The examiner can normally be reached on Monday-Friday 7:30a.m.-4:00p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.



A.W.
January 28, 2003



CHRISTINE T. TU
Primary Examiner